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MICHAEL O. SCHEINBERG
P.O. BOX 164140
AUSTIN, TX 78716-4140

EXAMINER	
TRIMMINGS, JOHN P	

ART UNIT	PAPER NUMBER
2133	3

DATE MAILED: 06/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/033,007	MCADAMS, MARK ALAN	
	Examiner	Art Unit	
	John P Trimmings	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☒ Claim(s) *1,3,4,16,19,23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 December 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 12.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-25 are presented for examination.

Information Disclosure Statement

The examiner has considered the references in the applicant's Information Disclosure Statement dated 5/20/2003.

Drawings

1. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: FIG.2 240. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. New corrected drawings are required in this application because hand-drawn entries should be professionally drawn. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to

the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Specification

4. The abstract of the disclosure is objected to because line 2 recites, "system of a chip", but the examiner believes it should read "system on a chip". Correction is required. See MPEP § 608.01(b).

5. The disclosure is objected to because of the following informalities: page 1 line 2 recites, "to testing of circuit module". Appropriate grammatical correction is required.

6. The disclosure is objected to because of the following informalities: page 4 last line recites, "are captured applied". Appropriate grammatical correction is required.

7. The disclosure is objected to because of the following informalities: page 5 line 11 recites, "input through a chip I/O pins". Appropriate grammatical correction is required.

8. The disclosure is objected to because of the following informalities: page 8 line 8 recites, "on circuit board". Appropriate grammatical correction is required.

Claim Objections

9. Claim 1 is objected to because of the following informalities: line 9 recites, "retrieving the output". Although the statement is understood, the examiner believes that since this is the first time an output of the circuit is recited, the phrase should read, "retrieving an output". Appropriate correction is required.

10. Claim 3 is objected to because of the following informalities: line 2 recites, "JTAG command", but the examiner believes that the phrase should read, "JTAG commands". Appropriate correction is required.

11. Claim 4 is objected to because of the following informalities: line 2 recites, "timing relationships", but the examiner believes that the phrase should read, "timing relationship". Appropriate correction is required.

12. Claim 16 is objected to because of the following informalities: line 3 recites, "including tri-state", but the examiner believes that the phrase should read, "including a tri-state". Appropriate correction is required.

13. Claim 19 is objected to because of the following informalities: line 6 recites, "the controller", but the examiner believes that the phrase should read, "the test controller". Appropriate correction is required.

14. Claim 23 is objected to because of the following informalities: line 6 recites, "scan register", but the examiner believes that the phrase should read, "scan registers". Appropriate correction is required.

15. Claim 23 is objected to because of the following informalities: line 9 recites, "when in the integrates circuit", but the examiner believes that the phrase should read, "when the integrated circuit". Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

16. Claim 10 recites the limitation "the selector" in line 2. There is insufficient antecedent basis for this limitation in the claim.

17. Claim 14 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claim instantiates 2 different latches, but then in line 4 recites "conveying data from the latch to the input pin". The claim is indefinite because the claim does not specify which latch conveys the data.

18. Claim 15 recites the limitation "the scan chain" in line 4. There is insufficient antecedent basis for this limitation in the claim.

19. Claim 17 recites the limitation "the test interface" in line 2. There is insufficient antecedent basis for this limitation in the claim.

20. Claim 19 recites the limitation "the boundary scan ring" in line 5 & 6. There is insufficient antecedent basis for this limitation in the claim.

21. Claims 1 and 25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The term "to a pin of the larger design" is first of all lacking antecedent basis, but is also indefinite because the language attempts to broadly infer to the integrated circuit as "the larger design". The examiner therefore rejects the claim as being indefinite, and recommends replacing the above quoted phrase with a phrase such as "to an outer pin of the integrated circuit".

22. Claim 25 recites the limitation "the inputs" in line 7. There is insufficient antecedent basis for this limitation in the claim.

23. Claim 25 recites the limitation "the scan chain" in line 9 & 10. There is insufficient antecedent basis for this limitation in the claim.

24. Claim 25 recites the limitation "the test interface" in line 10. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

25. Claims 1, 3-9, and 19-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Jaber, U.S. Patent No. 6028983.

As per Claim 1:

Jaber teaches a method of testing a circuit module embedded in an integrated circuit (see Abstract), at least some of the pins of the circuit module not being directly connected to a pin of the larger design, the method comprising: communicating test commands and data using a board-level test protocol through a test interface (column 4 lines 59-67 and column 5 lines 1-19) by; scanning test vector data into a scan chain

associated with the inputs of the circuit module (FIG.7 60, 62, 64, 66); applying the test vector data in the scan chain as input to the circuit module (FIG.7 68); and retrieving the output of the circuit module through the scan chain to the test interface (FIG.7 72, 74, 76 and column 4 lines 8-35).

As per Claim 3:

Jaber teaches the method of claim 1 further comprising converting a test vector into a series of JTAG protocol test commands and data, the JTAG command including a user defined command (FIG.5 44) for defining an address for a circuit module (column 6 lines 26-64).

As per Claim 4:

Jaber teaches the method of claim 3 in which converting a test vector includes maintaining timing relationships actions initiated by the test commands (see FIG.7 60-76).

As per Claim 5:

Jaber teaches the method of claim 1 in which scanning test vector data into a scan chain includes scanning the test vector data to a single boundary scan register (see Abstract), the single boundary scan register being associated with the circuit module under test (FIG.7 70).

As per Claim 6:

Jaber teaches the method of claim 1 in which retrieving the output of the circuit module through the scan chain to the test interface includes scanning the output of a boundary

scan register to the test interface without scanning the output through a second boundary scan ring (see Abstract and FIG.4).

As per Claim 7:

Jaber teaches the method of claim 1 in which retrieving the output of the circuit module through the scan chain to the test interface includes scanning the output of a boundary scan register through at least one dedicated output conductor (FIG.4 TDO).

As per Claims 8 and 19:

Jaber teaches A system for testing one or more of multiple circuit modules embedded in an integrated circuit (see Anstract), comprising: a test controller for accepting serial data and control signals from outside the integrated circuit in accordance with a test protocol that corresponds to a board level test protocol (FIG.5 39), the controller including; a first selector for selecting one of the multiple circuit modules for testing (FIG.5 47), control signals being transmitted to only the selected one of the test modulesFIG.5 49, 51); and a second selector for selecting output from the selected one of the circuit modules (FIG.5 53); and a boundary scan register corresponding to each of the one or more circuit modules (FIG.5 SCAN STRING 0...n), the boundary scan register providing input to circuit modules from the controller in a test mode and from an operating input when in operating mode (FIG.7 70 and FIG.6 DATA IN).

As per Claims 9 and 20:

Jaber teaches the system of claim 8 and 19 in which the test controller includes logic for using serial data and control signals in accordance with a JTAG protocol (column 4 lines 8-13).

As per Claim 21:

Jaber teaches the system of claim 19 in which the test controller includes a selector for selecting one of the multiple circuit modules for testing (FIG.5 47), control signals being transmitted to only the selected one of the test modules (FIG.5 49, 51 and Abstract).

As per Claim 22:

Jaber teaches the system of claim 19 in which a test controller for accepting serial data and control signals from a test interface in accordance with a test protocol that corresponds to a board level test protocol includes a selector for selecting output from the selected one of the circuit modules (FIG.5 53).

26. Claim 25 is rejected under 35 U.S.C. 102(e) as being anticipated by Bhattacharya, U.S. Patent No. 6425100. Bhattacharya teaches a method of testing a circuit module embedded in an integrated circuit design (see Abstract), at least some of the pins of the circuit module not being directly connected to a pin of the larger design (see Abstract), test commands and data being communicated to the circuit module using five conductors including a clock conductor (FIG.7 TCK), a test mode conductor (FIG.7 TMS), a reset conductor (FIG.7 TRST*), a data in conductor (FIG.7 TDI), and a data out conductor (FIG.7 TDO), the method comprising; scanning through the data in conductor (TDI) commands and data into a scan chain associated with the inputs of the

circuit module (FIG.7 725, 735); applying the data in the scan chain as input to the circuit module (FIG.7 TDI2); and retrieving through the data out conductor output of the circuit module through the scan chain (FIG.7 TDO2) to the test interface (FIG.7 TDO).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

27. Claims 2, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jaber, U.S. Patent No. 6028983, and further in view of Bhattacharya, U.S. Patent No. 6425100. Jaber teaches the method of claim 1 and system of Claim 8 in which communicating test commands and data includes communicating test commands and data from off the integrated circuit using four conductors including a clock conductor (FIG.5 TCK), a test mode conductor (FIG.5 TMS), a data in conductor (FIG.5 TDI) and a data out conductor (FIG.5 TDO). Jaber however fails to teach a fifth optional 1149.1

standard conductor, a reset conductor. In an analogous art, Bhattacharya teaches this feature (FIG.7 TRST*). One with ordinary skill in the art would find it to be an obvious choice to include the fifth conductor in a JTAG compatible interface as taught by Bhattacharya into the JTAG interface of Jaber, in order to maintain compliance and compatibility with IEE standard 1149.1. Bhattacharya, in column 1 lines 55-61 and column 2 lines 1-6 states the need to be JTAG compliant and an advantage of that invention as being compliant in that respect. One with ordinary skill in the art at the time of the invention, motivated by Bhattacharya, would combine the two references.

28. Claims 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jaber, U.S. Patent No. 6028983, and further in view of Jin, U.S. Patent No. 6266801. As per Claims 10 and 11:

Jaber teaches the system of claim 8 further comprising multiple sets of two conductors, one set connecting the selector to each of the boundary scan registers, as applied to LSSD design requirements. However, Jaber fails to teach distribution of four signals in this manner to comply with other master/slave scan register designs. In an analogous art, Jin does teach the feature, using multiple sets of four conductors (FIG.1C, MODE, SHIFTDR, CLOCKDR, UPDATEDR, as well as FIG.4). One with ordinary skill in the art would find it to be an obvious choice to include the four conductors in a master/slave arrangement as taught by Jin into the scan chain design of Jaber, in order to maintain compliance and compatibility with IEE standard 1149.1, and to also serve several embedded circuits. Jin, in column 2 lines 63-66 and column 2 lines 1-6 states the need and the advantage of an invention to be JTAG compliant without

impacting a circuit's timing characteristics. One with ordinary skill in the art at the time of the invention, motivated by Jin, would combine the two references, thus these claims are rejected.

As per Claim 12:

Jaber further teaches the system of claim 10 further comprising a data input line that connects from the test controller to every boundary scan register (FIG.5 TDI). And in view of the motivation previously stated above, the claim is rejected.

As per Claim 13:

Jaber further teaches the system of claim 10 further comprising multiple data output lines (FIG.5 SCAN STRING 0...n), each connecting from a different boundary scan register to the second selector (FIG.5 53). And in view of the motivation previously stated above, the claim is rejected.

29. Claims 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jaber, U.S. Patent No. 6028983, and further in view of Sim, U.S. Patent No. 6374380. Jaber further teaches the system of claim 8 in which each boundary scan register includes test logic for each input pin (FIG.5 47 and SCAN STRING 0...n) output pin (FIG.5 49, 51 and SCAN STRING 0...n), of the corresponding circuit module, the test logic for each input or output pin including a latch for scanning in data (FIG.5 m), and a latch for applying data (FIG.5 s). Jaber fails to teach a bi-directional pin (...) and a data selector for selectively conveying data from the latch to the input pin. In an analogous art, Sim teaches these features in FIG.8 (selector 66) and bi-directional circuit in FIG.11, as well as being a tri-state buffer (column 2 lines 45-48). One with ordinary skill in the

art would find it to be an obvious choice to add a bi-directional capability arrangement as taught by Sim into the scan chain design of Jaber, in order to maintain compliance and compatibility with IEE standard 1149.1, and to also serve several types embedded circuits, including bi-directional types. Sim, in column 2 lines 1-49 states the need and the advantage of an invention to be JTAG compliant without impacting a circuit's I/O pin overhead. One with ordinary skill in the art at the time of the invention, motivated by Sim, would combine the two references, thus the claim is rejected.

30. Claims 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jaber, U.S. Patent No. 6028983, in view of Bhattacharya, U.S. Patent No. 6425100, and further in view of Jin, U.S. Patent No. 6266801.

As per Claim 23:

Jaber teaches the system for testing one or more of multiple circuit modules embedded in an integrated circuit, comprising: a test controller for accepting serial data and control signals from outside the integrated circuit, using four conductors including a clock conductor (FIG.5 TCK), a test mode conductor (FIG.5 TMS), a data in conductor (FIG.5 TDI) and a data out conductor (FIG.5 TDO), one or more multiple boundary scan registers (FIG.5 SCAN STRING 0...n), each boundary scan register corresponding to one of the circuit modules (see Absract), each boundary scan register providing input to the corresponding circuit module from the test controller when the integrated circuit is in a test mode and from an operating input when in the integrates circuit is in an operating mode (FIG.7 70 and FIG.6 DATA IN). Jaber however fails to teach a fifth optional 1149.1 standard conductor, a reset conductor. In an analogous art, Bhattacharya

teaches this feature (FIG.7 TRST*). One with ordinary skill in the art would find it to be an obvious choice to include the fifth conductor in a JTAG compatible interface as taught by Bhattacharya into the JTAG interface of Jaber, in order to maintain compliance and compatibility with IEE standard 1149.1. Bhattacharya, in column 1 lines 55-61 and column 2 lines 1-6 states the need to be JTAG compliant and an advantage of that invention as being compliant in that respect. Jaber also teaches conductors for the test controller to communicate with the boundary scan registers, the conductors including a data-in line (FIG.5 TDI), a data-out line (FIG.5 TDO), a clock line (FIG.5 49), and an input application line to indicate that input data in the boundary scan register is to be applied to the inputs of the circuit module (FIG.5 51). Jaber fails to teach an two additional lines; a mode line to indicate whether the integrated circuit module is in test mode or operating mode, and an output data capture line indicating that output from the circuit module is to be captured. But in the analogous art of Jin, these two signals are featured in FIG.1C as MODE and UPDATEDR. One with ordinary skill in the art would find it to be an obvious choice to include the six conductors above in a master/slave arrangement as taught by Jin, into the scan chain design of Jaber, in order to maintain compliance and compatibility with IEE standard 1149.1, and to also serve several embedded circuits. Jin, in column 2 lines 63-66 and column 2 lines 1-6 states the need and the advantage of an invention to be JTAG compliant without impacting a circuit's timing characteristics. One with ordinary skill in the art at the time of the invention, motivated by Bhattacharya and Jin, would combine the two references.

As per Claim 24:

Jaber further teaches the method of claim 23 in which the test controller includes logic for accepting commands and data formatted in a JTAG protocol (see Abstract). And in view of the motivation previously stated, the claim is rejected.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P Trimmings whose telephone number is 703-305-0714. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John P Trimmings
Examiner
Art Unit 2133

Guy J. Lamarre
for

jpt

Albert DeCady
Primary Examiner